ABSTRACT

A computer processor integrated circuit has multiple functional units, where each unit is coupled to a register file for reading and writing operands. An instruction fetch unit receives instructions from a memory system and dispatches commands to the functional units. The processor has a resource status flags register wherein particular units may be marked enabled or disabled. The instruction fetch and decode unit checks the resource status flags register prior to dispatching commands and dispatches commands only to those functional units marked enabled. The instruction fetch and decode unit is capable of dispatching commands to available units, and of stalling and dispatching remaining commands in a following cycle if insufficient resources are available to simultaneously dispatch all commands necessary to execute an instruction or group of instructions.